

REMARKS

Claims 1-28, all the claims pending in the application, stand rejected under 35 U.S.C. §102(b) on prior art grounds. Claims 2-4, 10-11, and 17-19 stand rejected upon informalities under 35 U.S.C. §112, second paragraph. Applicants respectfully traverse these rejections based on the following discussion.

I. The 35 U.S.C. §112, Second Paragraph, Rejection

Claims 2-4, 10-11, and 17-19 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. While the Applicants respectfully traverse these rejections, claims 2-4, 10-11 and 17-19 are amended herein to further clarify the subject matter of the invention. Specifically, claims 2 and 17 are amended to reflect that the spacers are formed adjacent to the gate stack and, particularly, adjacent to both the gate conductor and the at least one sacrificial oxide layer above said gate conductor (see Figures 7A-7B). Thus, the height of the spacer is above the height of the gate conductor. As indicated in paragraphs [0008] and [0030-0031], the gate height limits the achievable size of the spacers. So, by artificially increasing the gate height with the sacrificial layer, larger spacers can be formed using a formation process for spacer width modulation. The larger spacers (i.e., spacers with a relatively larger width) allow more room for dopant diffusion when the source and drain regions are formed. Thus, claims 3, 10 and 18 have been amended to reflect that the size of the spacers is controlled by the height of the gate stack and by forming the gate stack from the gate conductor and the sacrificial layer, as

opposed to from the gate conductor alone, a height of the gate stack can be increased so that the size, including the width, of the spacers can be modulated to form larger spacers. Claims 4, 11, and 19 have been amended to reflect that forming the larger spacers positions the source and drain regions further from the gate conductor when compared to source and drain regions formed with spacers formed only to the height of the gate conductor. The claims 2-4, 10-11 and 17-19, as amended, particularly point out and distinctly claim the subject matter of the invention. Furthermore, claims 2-4, 10-11 and 17-19, as amended, are intended to neither narrow nor broaden the scope of the invention, as originally claimed. In other words, the claim language is changed so that the invention is more clearly understood, but the semantics are the same. Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. The Prior Art Rejections

Claims 1-28 stand rejected under 35 U.S.C. §102(b) as being anticipated by Park, et al. (U.S. Patent No. 6,429,084), hereinafter referred to as Park. Applicants respectfully traverse these rejections based on the following discussion. Specifically, regarding independent claim 1, Park does not teach or suggest doping regions of the substrate not protected by the spacers with a dopant to form source and drain regions adjacent the gate stack, wherein the spacers are formed with a target spacer width to minimize diffusion of the dopant into a channel region of the substrate below the gate conductor. Furthermore, regarding independent claims 9, 16 and 24, Park does not teach or suggest after epitaxially growing raised source and drain regions, implanting impurities into the raised

source and drain regions and into said substrate below the raised source and drain regions, wherein implanting the impurities after epitaxially growing the raised source and drain regions avoids subjecting the impurities to the thermal budget of the epitaxially growing process and wherein the spacers are formed with the target spacer width to minimize diffusion of the impurities into the gate conductor.

While the cited prior art and the present invention each provide methods for forming CMOS transistors with raised source and drain regions and each address problems associated with reduced height of gate conductors, the problems addressed are different as are the processes used to solve the problems. More particularly, as mentioned in the background paragraphs [0001-0006] of the specification of the present invention, and particularly, in paragraph [0004], with increased scaling of CMOS structures implanting dopants with sufficient energy to dope the source and drain regions and for halo formation using the poly gate as a self-aligned mask can cause the dopants to penetrate through the poly gate and the gate dielectric into the channel as the gate height is decreased. To avoid this, some conventional processes reduce the total thermal budget of the manufacturing processes. Additionally, as mentioned in paragraph [0005], the maximum sidewall spacer length (i.e., width) achievable with a gate of reduced height poses challenges. With the shorter gate height, the maximum sizes of the spacer is reduced due to the reduced step height for reactive ion etch of a deposited spacer material of a given thickness, resulting in lateral encroachment of S/D dopants, and a higher probability of silicide bridging between the gate and the S/D. This problem becomes more severe when using epitaxially grown raised source and drain structures because

epitaxial overgrowth occurs on top of the gate with reduced height. The undesirably overgrown epitaxial polysilicon over the gate would also be silicided which would form a conductive path between the gate and the raised source/drain regions, resulting in failure of transistor function.

Park addresses the problem of unwanted overgrown epi growth on the gate and STI but not unwanted diffusion of dopants. Specifically, Park discloses a method of forming CMOS transistors with raised source and drain regions (col. 1, lines 5-6) in which a protective layer is provided over the gate and the STI (col. 1, lines 26-29). In the Park method a gate stack is formed with several sacrificial layers above a gate conductor (col. 1, lines 58-62). The sacrificial layers protect the surface of the gate conductor during subsequent processing. A protective nitride layer is deposited over the substrate, gate stack, and the STI structures (col. 1, lines 66-67). Temporary spacers are formed against the gate stack and a width of the spacers is set to define the area for the halo and extensions implants (col. 2, lines 1-5). A portion of the nitride layer is etched to above the substrate to define the source and drain regions and the temporary spacers are removed (col. 2, lines 25-30). Then, the source and drain regions in the substrate are implanted (col. 2, lines 33-34; see Figure 5). After the source and drain regions in the substrate are implanted, raised source and drain regions are epitaxially grown (col. 2, lines 43-47; see Figure 7). Unwanted epi growth is prevented by the remaining nitride layer. Then, after additional processing steps, extension and halo implantation is performed (col. 2, lines 48-64), which also implants the raised epitaxially grown source and drain regions.

Park does not address the problem caused by dopants penetrating through the poly gate and the gate dielectric into the channel as the gate height is decreased. Specifically, as mentioned above, Park discloses the formation of temporary spacers adjacent the gate stack; however, the width of the temporary spacers is set to define the area for the halo and extensions implants. The Applicants respectfully submit that Park does not teach or suggest forming spacers with a target spacer width (see paragraph [0036]), wherein the spacers are formed with the target spacer width to minimize diffusion of the dopant into a channel region of the substrate below the gate conductor, as claimed in claim 1, or to minimize diffusion of the impurities into the gate conductor as claimed in claims 9, 16, and 24 (see paragraphs [0029-0031] and [0039]). Furthermore, regarding independent claims 9, 16 and 24, Park does not teach or suggest after epitaxially growing raised source and drain regions, implanting impurities into the raised source and drain regions and into said substrate below the raised source and drain regions, wherein implanting the impurities after epitaxially growing the raised source and drain regions avoids subjecting the impurities to the thermal budget of the epitaxially growing (see paragraphs [0042] and [0047]). Specifically, Park discloses implanting the source and drain regions in the substrate before epitaxially growing the raised source and drain regions (col. 2 lines 33-48). The impurities implanted into the source and drain region would necessarily be subjected to the epi process (with a conventional temperature range from about 750°C-850°C) and, thus, deleterious effects of transient enhanced diffusion of impurities, such as boron, would not be avoided.

Applicants respectfully submit that independent claims 1, 9, 16, and 24 are patentable over the prior art of record. Further, dependent claims 2-8, 10-15, 17-23 and 25-28 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

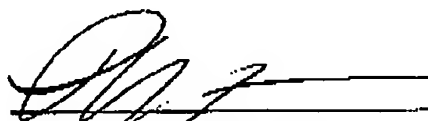
With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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